

AL460A HD-FIFO Module

Fulfill your high speed video buffering needs!

High-Speed First-In-First-Out memory buffer for HD Video applications

Introduction

The AL460A HD-FIFO Modules are used to facilitate development of products using the AL460A HD-FIFO IC chips, which are used in HD Video applications as important memory buffering technology. These modules are also used to validate and benchmark the AL460A chip functionality and performance.

The AL460A HD-FIFO modules allow a maximum 4.8 Gbps data throughput and are designed with Dual Embedded AL460A-7-PBF (or AL460A-13-PBF) chips to demonstrate the full potential of HD-FIFO technology. Dual chips, working in parallel, can turn over very dense HD Video data efficiently by expanding the bus width to 32-bits, while running at a maximum clock rate of 150 MHz. Control signals and data bus signals on the module are clearly demarcated on two 50-pin connectors; one connector is reserved for write controls and the input data bus; the other connector is for read controls and the output data bus.

The AL460A is designed with a straightforward bus interface, reducing implementation and debugging efforts, and helping customers develop faster and more efficiently. This board is especially designed and optimized to be easily integrated as an add-on module on existing systems, significantly reducing interface engineering issues commonly found in retrofit efforts. This allows designers the luxury of being able to focus on core functionality and product quality.

AL460A HD-FIFO Advantages

HD-FIFO is a proprietary design technology used to overcome issues commonly hindering and limiting other frame buffer devices (e.g. SDRAM, DDR...etc) found in FPGA solutions. Traditional FPGA implementations require higher I/O pin totals and place heavy demands on logic resources and property memory controllers, forcing a designer to move up to higher grade FPGAs. In contrast, AverLogic's HD-FIFO requires significantly less in I/O pins and logic resources, at the same time overcoming latency issues therein. The programmable I/O controls and double buffer mode increase design flexibility and reduce FPGA overhead.

A straightforward developer interface saves time in overall design and debugging efforts, allowing you to save costs and speed up your time-to-market.

Applications

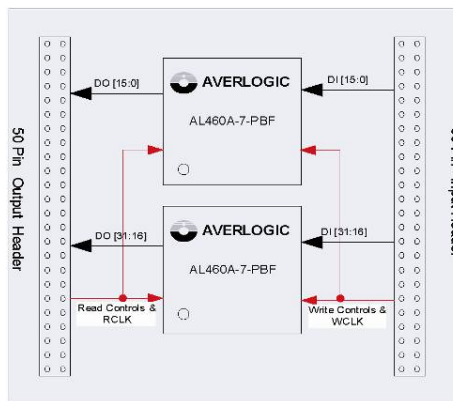
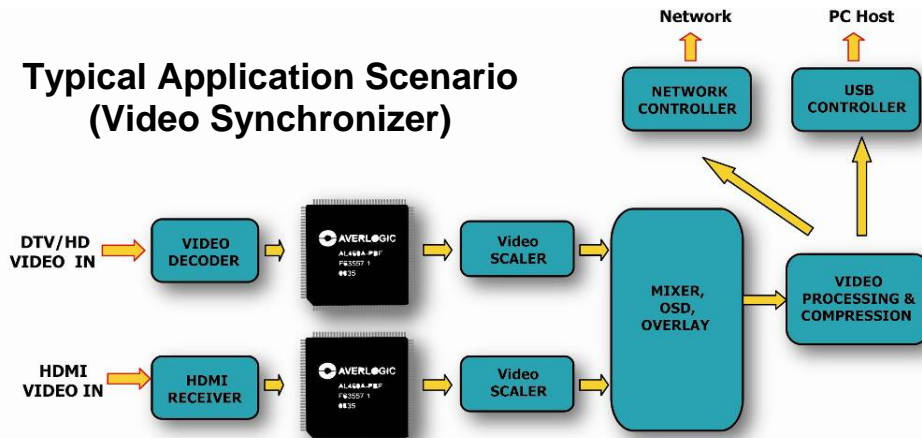
- HD video capturing and editing systems
- Switcher or format converter box
- Scan rate converters
- Time base correction (TBC)
- Frame synchronizer
- HD digital video camera buffering

Module Specifications (The AL460 Module is RoHS compliant)

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| <ul style="list-style-type: none">■ AL460A-7(-13)-PBF (x2)■ Dimensions: 80 mm x 80 mm■ Configuration - Parallel AL460A chips provide a 32-bit I/O bus■ Clock - 14.31818 MHz on-board Crystal | <ul style="list-style-type: none">■ Connectors - Low profile 25x2 2.0 mm male header (x2)■ Up to 1080p video stream data■ Power and analog device - 3.3V input from existing system or external power supply. 2.5V Ultra low dropout linear regulator LP3852. |
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General Features

- 256 Mbit density, 8M x 32-bit FIFO memory
- Maximum 150 MHz, 32-bit synchronous sequential read/write operations
- Maximum 4.8 Gbps throughput
- 3.3V power supply
- Programmable I/O control
- Supports double buffer mode (4M x32-bit upper and lower frames access)
- Selectable Polarity control

Block Diagrams
AL460 module Block Diagram

**Typical Application Scenario
(Video Synchronizer)**

Ordering Information

Part number	Speed	Data Bus	Power
DST-0106A-MDL-A0	150 MHz	32-bit	+3.3V
DST-0106A-MDL-A1	75 MHz	32-bit	+3.3V